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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/388,031	09/01/1999	SALMAN AKRAM	3442US(96-42	3303

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EXAMINER	
LEE, EUGENE	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/388,031	AKRAM, SALMAN`	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 100-129* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 100-129* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/3/03 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 16, 23, 101, 116, 123 and 129 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. 6,153,900. Chang discloses (see, for example, FIG. 6) a metallization structure comprising a substrate 10, metal layer 16, conductive line 24, dielectric layer 18, metal spacer 20a/22a, and conductive layer 28. The substrate has an overlying metal layer 16 wherein the metal layer 16 underlies the conductive line 24. The dielectric layer 18 has an aperture 14 formed therein with sidewalls exposing the metal layer 16. Metal spacers are formed on the sidewalls of dielectric layer 18 and contact the metal layer 16.

The conductive layer 28 is in contact with the top surface of metal spacers 22a and together substantially fill the aperture 14. The upper surface of conductive layer 28 over the aperture 14 is at the same level (coincident) as the upper surface of the dielectric layer 18.

Regarding the material of layer 16, see, for example, column 6, lines 2-3 wherein Chang states the layer as a metal polyside.

Regarding whether the material of the spacer, see, for example, column 6, lines 32-37 wherein Chang states the first conductive layer (which eventually becomes the spacer) 20 as metal poly-silicide or aluminum alloy.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4 thru 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan et al. 6,074,943 in view of Liu et al. 6,277,745 B1. Brennan discloses (see, for example, FIG. 3) an interconnect structure comprising an underlying layer (substrate) 300, interconnect (single conducting layer) 310, and a thick buffer region (spacers) 320. In column 1, lines 33-39, Brennan discloses that the thick buffer region may be metal. Brennan does not disclose a metal layer defining a pattern on a portion of the substrate upper surface. However, Liu shows (see, for example, FIG. 1D) an interconnect structure wherein a bottom barrier layer (metal layer) 4 lies underneath a copper interconnect layer 6. The bottom barrier layer passivates

the underside of the copper interconnect layer. See, for example, column 3, lines 34-38. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the bottom barrier layer of Liu in Brennan's invention in order to passivate the bottom surface of the interconnect.

Regarding claims 4 and 5, Liu states (see, for example, column 3, lines 38-42) that the bottom barrier layer may comprise TaN, TiN, Ta, or various single or stacked combinations.

Regarding claim 8, Brennan does not disclose the interconnect as copper or aluminum. However, Liu states (see, for example, column 1, lines 11-45) that copper is a material used for interconnects, which provides better circuit speed than aluminum. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use copper in the interconnect material of Brennan in order to have good circuit speed and therefore minimize signal delays within a circuit.

Regarding claim 9, Brennan in view of Liu does not disclose the single conductive layer being an aluminum-copper alloy. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use an aluminum-copper alloy, since aluminum-copper alloy has excellent conductive properties and it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims 10 and 11, Brennan does not disclose the metal spacers comprising at least one of Ti, Ta, W, Co, or Mo, or alloys thereof or compounds thereof, including TaN and TiN. However, Liu describes (see, for example, column 4, lines 24-29) an interconnect structure comprising protective spacers wherein the protective spacers may comprise Ta, TaN, TiN, or

combinations thereof. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use these materials in the metal spacers of Brennan in order to adequately protect the sidewalls of the interconnect structure.

Regarding claim 12, Brennan does not disclose the a dielectric layer on the conducting layer and having sidewalls aligned with said sidewalls of the single conducting layer, the metal spacers extending along the sidewalls of the dielectric layer. However, Liu teaches (see, for example, column 5, lines 1-17) an insulating layer (dielectric layer) 16 that insulates the top surface of the interconnect structure. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the insulating layer of Liu in Brennan in order to insulate and protect the top of the interconnect structure.

6. Claims 2, 3, 100, 102 thru 113 and 115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan et al. '943 in view of Liu et al. '745 as applied to claims 1, 4 thru 13, and 15 above, and further in view of Cox 6,166,439. Brennan in view of Liu does not disclose a dielectric layer on the substrate upper surface and underlying the metal layer. However, Cox discloses (see, for example, Fig. 2) a semiconductor device comprising conductive lines 54, 56, and 58 over an insulating layer 50a and substrate 50b. The insulating layer serves as a base upon which the conductive pattern is constructed. See column 5, lines 1-7. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the insulating layer in order to provide a further base for the semiconductor device.

Regarding claims 3 and 103, Brennan in view of Liu in view of Cox does not disclose the dielectric layer being silicon oxide or BPSG. However, it would have been obvious to one of

ordinary skill in the art at the time of invention was made to use silicon oxide or BPSG, since silicon oxide and BPSG provide strong insulative properties and it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 109, Brennan in view of Liu in view of Cox does not disclose the single conductive layer being an aluminum-copper alloy. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use an aluminum-copper alloy, since aluminum-copper alloy has excellent conductive properties and it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan et al. '943 in view of Liu et al. '745 as applied to claims 1, 4 thru 13, and 15 above, and further in view of Matsuno 6,046,502. Brennan in view of Liu does not disclose a fluorine-doped silicon oxide. However, Matsuno teaches that dielectric films doped with fluorine provide films with low dielectric constants. See, for example, see column 1, lines 20-63. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to add fluorine, in order to form a low dielectric film, and improve the overall speed of a semiconductor device.

8. Claims 17, 18, 24, 25, 117, 118, 124, and 125 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '900 as applied to claims 16, 23, 116, and 123 above, and

further in view of Chang 5,712,195. Chang '900 does not disclose the metal layer comprising tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN. However, Chang '195 discloses (see, for example, column 4, lines 7-14) a metallization structure comprising a conductive layer (metal layer) formed by depositing titanium tungsten. Chang '195 discloses that this formation of the conductive layer is one of many well-known conventional techniques. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN in the metal layer of Chang '900 in order to form a conductive line with adequate conductive properties.

9. Claims 19, 20, 119, and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '900 as applied to claims 16, 23, 101, 116, 123 and 129 above, and further in view of Lee 6,242,340 B1. Chang does not disclose the metal spacer including at least one layer of metal comprising tantalum, titanium, tungsten, cobalt, molybdenum, or alloys or compounds thereof, including TaN and TiN. However, Lee discloses (see, for example, FIG. 3D) a metallization structure comprising sidewall spacers 36a. In column 4, lines 42-44, Lee states the sidewall spacers comprise TiN, Ta, TaN, WNx and combinations thereof. The sidewall spacers protect the sidewalls of the insulation layer 32 and prevent the second interconnection layer 40 from diffusing out of the trench 32. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include tantalum, titanium, tungsten, cobalt, molybdenum, or an alloy or a compound of any thereof, including TaN and TiN in order to

protect the sidewalls of first insulating layer and prevent the second conductive layer from diffusing in Chang's invention.

10. Claims 21, 22, 121, and 122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '900 as applied to claims 16, 23, 101, 116, 123 and 129 above, and further in view of Cox '439. Chang does not disclose the substrate comprising a dielectric layer underlying the metal layer. However, Cox discloses (see, for example, Fig. 2) a semiconductor device comprising conductive lines 54, 56, and 58 over an insulating layer 50a and substrate 50b. The insulating layer serves as a base upon which the conductive pattern is constructed. See column 5, lines 1-7. The insulating layer also provides suitable separation between the overlying semiconductor device and the substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the insulating layer on the substrate of Liu for the reasons cited above.

11. Claims 26 thru 28 and 126 thru 128 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '900 as applied to claims 16, 23, 101, 116, 123 and 129 above, and further in view of Naik '380. Chang does not disclose the at least one upper metal layer on the conductive layer comprising Ti, Ta, W, Co, or Mo or an alloy or a compound of any thereof, including TaN or TiN. However, Naik discloses (see for example, FIG. 3F and column 5, lines 57-58) a metallization structure comprising a titanium liner 318. This liner provides electrical conductance to the metal line 302. Therefore it would have been obvious to one of ordinary skill

in the art at the time of invention to use titanium in Chang's invention in order to have metal layer with high electrical conductance next to the interconnection layer.

12. Claim 114 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan et al. '943 in view of Liu et al. '745 in view of Cox '439 as applied to claims 2, 3, 100, 102 thru 113 and 115 above, and further in view of Matsuno '502. Brennan in view of Liu in view of Cox does not disclose a fluorine-doped silicon oxide. However, Matsuno teaches that dielectric films doped with fluorine provide films with low dielectric constants. See, for example, see column 1, lines 20-63. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to add fluorine, in order to form a low dielectric film, and improve the overall speed of a semiconductor device.

Response to Arguments

13. Applicant's arguments with respect to claims 1-28, and 100-129 have been considered but are moot in view of the new ground(s) of rejection.

Regarding applicant's argument on page 14, fourth paragraph of amendment filed 11/3/03 that the conductive layer 28 does not have an upper surface coincident with an upper surface of said dielectric layer, this argument is not persuasive. In FIG. 6, Chang discloses the conductive layer 28 coincident with an upper surface of dielectric layer 18. Looking at the upper surface of the conductive layer 28 over aperture 14, the upper surface is clearly at the same level (coincident) as the dielectric layer 18. This is the same coincidence that is shown in the

applicant's figures wherein applicant discloses (see, for example, FIG. 8) a conductive layer 66 having an upper surface substantially coincident with an upper surface of said dielectric layer 54.

Regarding applicant's argument on the top of page 15 that, by contrast, Chang discloses conductive layer 24 out of contact with spacer 22a and conductive layer 28 does not have an upper surface coincident with an upper surface of dielectric layer 18 (this argument has already been addressed), nor does conductive layer 28 and metal spacer 22 substantially fill the aperture in 18, this argument is not persuasive. In FIG. 6, Chang clearly discloses the conductive layer 28 being in contact with a top surface of spacers 22a. The conductive layer 28 is not out of contact with spacer 22a. Regarding whether conductive layer 28 and metal spacer 22 substantially fill the aperture in dielectric layer 18, this is shown in FIG. 6 of Chang. The aperture that was formed in dielectric layer 18 is clearly filled by the conductive layer 28 and metal spacers 22a.

On page 17, first paragraph, applicant argues that FIG. 3 of Brennan is an intermediate product and that Brennan does not expressly teach that the upper layer of interconnect 310 being out of contact with any metal. However, this argument is not persuasive. In FIG. 3, Brennan clearly discloses the final structure of a prior art interconnect structure. There is no description of intermediate structures regarding this interconnect structure.

FIG. 3 of Brennan does not show any metal contacting the interconnect 310, therefore, Brennan clearly discloses no metal contacting the interconnect 310.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
February 24, 2004

Tom Thomas
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